REMARKS

Claims 1-6 and 13-17 are pending in the Application. Claims 1-6 are rejected under 35 U.S.C. § 103(a). Claims 13-17 are allowed. Claim 18 has been added and hence claims 1-6 and 13-18 are pending in the Application. Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

I. REJECTIONS UNDER 35 U.S.C. § 103(a):

The Examiner has rejected claims 1-6 under 35 U.S.C. § 103(a) as being unpatentable over Chung et al. (U. S. Patent No. 6,184,142) (hereinafter "Chung") in view of Applicants' Background. Applicants respectfully traverse these rejections for at least the reasons provided below and respectfully request the Examiner to reconsider and withdraw these rejections.

A. Chung and Applicants Background, taken singly or in combination, do not teach or suggest the following limitations.

Applicants respectfully assert that Chung and Applicants' Background, taken singly or in combination, do not teach or suggest "providing an antireflective coating (ARC) layer having antireflective properties, wherein the ARC layer comprises a layer of SiON having a thickness of less than about 500 Angstroms (Å) deposited on the first layer" as recited in claim 1 and similarly in claim 18. The Examiner states that Chung does not disclose an ARC layer having a thickness of less than about 500 Angstroms. Paper No. 8, page 3. The Examiner further states:

> However, the selection of the ARC layer thickness is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. *In re Jones*, 162 U.S.P.Q. 224 (C.C.P.A. 1955) (the selection of optimum ranges within prior art general conditions is obvious) and *In re Boesch*, 205 U.S.P.Q. 215 (C.C.P.A. 1980) (discovery of optimum value of result effective variable in a known process is obvious). For example, the thickness is a consideration of optimizing an antireflective property for etching purpose, as

> evidenced by AAPA, wherein the ARC layer is typically 300 Angstroms plus or minus 30 Angstroms (pages 1-2). Paper No. 8, page 3.

Applicants respectfully assert that the Examiner is misguided by relying upon *In re Jones* and *In re Boesch* in support of the assertion that the selection of an ARC layer with a thickness of 500 Angstroms is obvious because it is a matter of determining optimum process condition by routine experimentation. Instead, these cases stand for the proposition that when the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum workable ranges by routine experimentation. M.P.E.P. § 2144.05; *In re Aller*, 220 F.2d 454, 456, 105 U.S.P.Q. 233, 235 (C.C.P.A. 1955). The Examiner has not cited any passage in Chung that teaches any range of thickness' that cap layer 114 (the Examiner asserts that cap layer 114 teaches an ARC layer). Further, the Examiner has not cited a passage in Chung containing language related to a thickness of cap layer 114. Since Chung does not contain any language that teaches a thickness of cap layer 114, the reliance upon *In re Jones* and *In re Boesch*, to support the proposition that an optimum process condition may be determined by routine experimentation is in error.

Further, Applicants note that *In re Jones*, upon which the Examiner relies, precedes *Graham v. John Deere Co.*, 383 U.S. 1, 148 U.S.P.Q. 459 (1966). Accordingly, the holdings of *Graham* may overrule the holdings of *In re Jones*.

Therefore, the Examiner has not provided a *prima facie* case of obviousness for rejecting claims 1 and 18. M.P.E.P. § 2143.

Applicants further assert that Chung and Applicants' Background, taken singly or in combination, do not teach or suggest "patterning a resist layer, the resist layer including a pattern having a plurality of apertures therein for etching a first portion of the first layer" as recited in claim 1 and similarly in claim 18. The Examiner cites resist layer 130 as teaching a resist layer including a pattern having a plurality of apertures. Paper No. 8, page 2. Applicants respectfully traverse and assert that resist

layer 130 has a single aperture and not a plurality of apertures as illustrated in Figure 6A. Therefore, the Examiner has not presented a *prima facie* case of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Chung and Applicants Background, taken singly or in combination, do not teach or suggest "removing the resist layer utilizing a plasma etch, the ARC layer being resistant to the plasma etch" as recited in claim 1 and similarly in claim 18. The Examiner recites to Figures 6A-6B as teaching the above-cited claim limitation. Paper No. 8, page 3. Applicants respectfully traverse and assert that Chung instead teaches that photoresist layer 130 is removed by using O_2 plasma treatment. However, there is no language in Chung that cap layer 114 (the Examiner asserts that cap layer 114 teaches an ARC layer) is resistant to the O_2 plasma treatment. The Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Chung to have cap layer 114 resistant to a plasma etch. Since the Examiner has not provided any evidence for modifying Chung to have cap layer 114 be resistant to a plasma etch, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 1. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Applicants further assert that Chung and Applicants' Background, taken singularly or in combination, do not teach or suggest "removing said first resist layer utilizing a plasma etch after said first portion of said first layer is etched" as recited in claim 18. Instead, Chung teaches that the hole pattern of cap layer 114 is transferred into two low k organic layers 112 and 113 (where the Examiner asserts that low k organic dielectric layer 113 corresponds to a first layer cited in claim 18), including stop layer 116 after the photoresist layer 130 (the Examiner asserts that photoresist layer 130 corresponds to a first resist layer as recited in claim 18) is removed. Column 4, lines 44-54. Therefore, the Examiner has not presented a *prima facie* case

of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Claims 2-6 each recite combinations of features including the above combinations, and thus are patentable for at least the above stated reasons. Claims 2-6 recite additional features, which, in combination with the features of the claims upon which they depend, are patentable over Chung in view of Applicants' Background.

For example, Chung and Applicants' Background, taken singly or in combination, do not teach or suggest "performing the plasma etch using a plasma including a forming gas, the ARC layer being resistant to the plasma etch using the plasma including the forming gas" as recited in claim 3. The Examiner has not cited any passage in either Chung or Applicants' Background as teaching or suggesting performing a plasma etch that removes a resist layer where the plasma etch uses a plasma including a forming gas. Further, the Examiner has not cited to any passage in either Chung or Applicants' Background that teach or suggest that the ARC layer is resistant to the plasma etch using the plasma including the forming gas. Since the Examiner has not cited to any passage, and since the Examiner has not provided any objective evidence for modifying Chung to perform a plasma etch on photoresist layer 130 using a plasma including the former gas where cap layer 114 is resistant to such a plasma etch, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 3. M.P.E.P. § 2143; *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Applicants further assert that Chung and Applicants' Background, taken singularly or in combination, do not teach or suggest "wherein the plasma further includes four percent of the forming gas" as recited in claim 4. The Examiner states that Chung does not teach this limitation. Paper No. 8, page 4. The Examiner further states:

> However, the selection of the percentage of the forming gas is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. *In re Jones*, 162 U.S.P.Q. 224 (C.C.P.A. 1955) (the selection of optimum ranges within prior art general conditions is obvious) and *In re Boesch*, 205 U.S.P.Q. 215 (C.C.P.A. 1980) (discovery of optimum value of result effective variable in a known process is obvious). In such a situation, Applicants must show that the particular range is critical, generally by showing that the claim range achieved unexpected results. *See* M.P.E.P. § 2144.05 III. In fact, the originally filed Specification does not demonstrate any criticality and/or novelty as to why the forming gas has to be four percent. Paper No. 8, page 4.

Again, as stated above, the Examiner is misguided in relying upon *In re Jones* and *In re Boesch* as well as M.P.E.P. § 2144.05, as Chung does not teach any percentage of a forming gas. Instead, as stated above, these cases stand for the proposition that when the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum workable ranges by routine experimentation. M.P.E.P. § 2144.05; *In re Aller*, 220 F.2d 454, 456, 105 U.S.P.Q. 233, 235 (C.C.P.A. 1955). Since the Examiner has not cited to any passage in Chung as teaching any percentage of a forming gas, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 4. M.P.E.P. 2144.05. Further, since the Examiner has not provided a *prima facie* case of obviousness based on overlapping ranges, Applicants do not have to rebut the Examiner's case by showing the criticality of plasma including four percent of the forming gas. M.P.E.P. § 2144.05 III. Hence, in view of the remarks stated above, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 4. M.P.E.P. § 2143.

Applicants further assert that Chung and Applicants' Background, taken singly or in combination, do not teach or suggest "providing a wet preclean after the plasma etching step" as recited in claim 5. The Examiner states the Chung does not teach the above-cited claim limitation. Paper No. 8, page 4. The Examiner further states that Applicants' Background teaches the above-cited claim limitation. Paper No. 8,

page 4. Applicants respectfully traverse the assertion that Applicants' Background teaches the above-cited claim limitation. There is no language in Applicants' Background of removing a resist layer using a plasma etch. Hence, there is no language in Applicants' Background of teaching providing a wet preclean after removing the resist layer utilizing a plasma etch. Therefore, the Examiner has not presented a *prima facie* case of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Further, since the Examiner has not presented any objective evidence for modifying Chung to provide a wet preclean after etching photo resist layer 130 using O_2 plasma treatment, the Examiner has not provided a *prima facie* case of obviousness for rejecting claim 5. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Applicants further assert that Chung and Applicants' Background taken singly or in combination, do not teach or suggest "wherein a thickness of the SiON ARC layer is three hundred Angstroms plus or minus no more than approximately ten percent" as recited in claim 6. The Examiner states that Chung does not disclose an ARC layer with a thickness of three hundred Angstroms plus or minus approximately ten percent. Paper No. 8, page 3. The Examiner further states:

> However, the selection of the ARC layer thickness is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. *In re Jones*, 162 U.S.P.Q. 224 (C.C.P.A. 1955) (the selection of optimum ranges within prior art general conditions is obvious) and *In re Boesch*, 205 U.S.P.Q. 215 (C.C.P.A. 1980) (discovery of optimum value of result effective variable in a known process is obvious). For example, the thickness is a consideration of optimizing an antireflective property for etching purpose, as evidenced by AAPA, wherein the ARC layer is typically 300 Angstroms plus or minus 30 Angstroms (pages 1-2). Paper No. 8, page 3.

As stated above, Applicants respectfully assert that the Examiner is misguided by relying upon *In re Jones* and *In re Boesch* in support of the assertion that the selection of an ARC layer with a thickness of three hundred Angstroms plus or minus approximately ten percent is obvious because it is a matter of determining optimum process condition by routine experimentation. Instead, as stated above, these cases stand for the proposition that when the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum workable ranges by routine experimentation. M.P.E.P. § 2144.05; *In re Aller*, 220 F.2d 454, 456, 105 U.S.P.Q. 233, 235 (C.C.P.A. 1955). The Examiner has not cited any passage in Chung that teaches any range of thickness' that cap layer 114 (the Examiner asserts that cap layer 114 teaches an ARC layer). Further, the Examiner has not cited a passage in Chung containing language related to a thickness of cap layer 114. Since Chung does not contain any language that teaches a thickness of cap layer 114, the reliance upon *In re Jones* and *In re Boesch*, to support the proposition that an optimum process condition may be determined by routine experimentation is in error.

Further, Applicants note that *In re Jones*, upon which the Examiner relies, precedes *Graham v. John Deere Co.*, 383 U.S. 1, 148 U.S.P.Q. 459 (1966). Accordingly, the holdings of *Graham* may overrule the holdings of *In re Jones*.

Therefore, the Examiner has not provided a *prima facie* case of obviousness for rejecting claim 6. M.P.E.P. § 2143.

As a result of the foregoing, Applicants respectfully assert that there are numerous claim limitations not taught or suggested in the cited prior art, and thus the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-6 and 18.

B. The Examiner has not presented any objective evidence for combining Chung with Applicants' background.

A *prima facie* case of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all

of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

In order to reject under 35 U.S.C. § 103, therefore, the Examiner must provide a proper motivation for combining or modifying the references. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457-1458 (Fed. Cir. 1998); M.P.E.P. § 2142. The Examiner's motivation for modifying Chung with Applicants' Background to have an ARC layer that comprises a layer of SiON having a thickness of less than about 500 Angstroms, as recited in claim 1 and similarly in claim 18, is to "provide a suitable antireflective property for etching purpose." (Paper No. 8, page 3.) This motivation is insufficient to support a *prima facie* case of obviousness since it is merely the Examiner's own subjective opinion.

Chung teaches a simplified method for etching low k organic dielectric film. Abstract. Chung further teaches a substrate is provided with a hardmask layer and low k organic dielectric layer formed thereon in which the hardmask layer is on the dielectric layer. Abstract. Chung further teaches a layer of photoresist is formed on the hardmask layer and imaged with a pattern by exposure through a dark field mask. Abstract. Chung further teaches that as a key step, the pattern is transferred into the hardmask layer by dry etching and then the photoresist is stripped in-situ. Abstract. Chung further teaches that the interconnect is then formed by using dry etching the low k organic dielectric layer using the hardmask layer as a mask, and readying it for the next semiconductor process. Abstract. Chung further teaches that is an object of this invention to overcome the integration issues from conventional damascene etching for organic silicon-oxide films. Column 2, lines 37-39. Damascene is

defined by Semiconductor OneSource as a process in which interconnect metal lines are delineated in dielectrics isolating them from each other not be means of lithography and etching, but by means of chemical-mechanical planarization (CMP). Exhibit A.

Applicants' Background, on the other hand, teaches a conventional method for processing a portion of a conventional semiconductor device such as a conventional embedded flash memory. Specification, page 1, lines 13-14.

The Examiner must submit objective evidence and not rely on his own subjective opinion in support of combining the reference (Chung) that teaches a method for etching low k organic dielectric film with a reference (Applicants' Background) that teaches a conventional method for processing a portion of a conventional semiconductor device such as a conventional embedded flash memory. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). As the Examiner has not provided any objective evidence, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-6 and 18. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Chung to provide an ARC layer that comprises a layer of SiON having a thickness of less than about 500 Angstroms. *Id.* There is no suggestion in Chung of having cap layer 114 (Examiner asserts that cap layer 114 teaches the limitation of an ARC layer) having a particular thickness. As the Examiner has not provided any objective evidence, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-6 and 18. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Chung to provide a suitable antireflective property for etching purposes (Examiner's motivation). *Id.* There is no suggestion in Chung that cap layer 114 (Examiner asserts that cap layer 114 teaches the limitation of an ARC layer) should be modified to provide a suitable antireflective property for etching purposes. Consequently, the Examiner's motivation is insufficient to support

a *prima facie* case of obviousness for rejecting claims 1-6 and 18 since it is merely the Examiner's subjective opinion. *Id.*

C. The Examiner has not presented a reasonable expectation of success when combining Chung with Applicants' Background.

The Examiner must present a reasonable expectation of success in combining Chung with Applicants' Background in order to establish a *prima facie* case of obviousness. M.P.E.P. § 2143.02. Chung teaches a method for etching low k organic dielectric film in a semiconductor device that substantially avoids the complicated process flow from spin-on low k organic dielectric layer. Column 2, lines 32-36. Applicants' Background, on the other hand, teaches a conventional method for processing a portion of a conventional semiconductor device such as a conventional embedded memory. There is no language in Chung that suggests that the damascene process as taught in Chung would be used in connection with a conventional method for processing a portion of a conventional semiconductor device such as a conventional embedded flash memory. As stated above, a damascene may be defined as a process in which interconnect metal lines are delineated in dielectrics isolating them from each other not by means of lithography and etching, but by means of chemical-mechanical polarization. Instead, the Examiner's motivation appears to have been gleaned from Applicants' disclosure. Any judgment of obviousness must not include knowledge gleaned only from Applicants' disclosure. *In re McLaughlin*, 170 U.S.P.Q.2d 209, 212 (C.C.P.A. 1979). The Examiner has not presented any evidence that there would be a reasonable expectation of success in combining Chung with the Applicants' Background. Hence, the Examiner has not presented a sufficient basis for a reasonable expectation of success. Consequently, the Examiner has not provided a *prima facie* case of obviousness for rejecting claims 1-6 and 18. M.P.E.P. § 2143.02.

D. By combining Chung with Applicants' Background, the principle of operation of Chung would change.

If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959). Further, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). For the reasons discussed below, Applicants submit that by combining Chung with Applicants' Background, the principle of operation in Chung would change and subsequently render the operation in Chung to perform its purpose unsatisfactorily.

Chung teaches two low k organic dielectric layers 112 and 113, stop layer 116 and cap layer 114 are formed using any suitable method and all their thickness will take appropriate values. Column 4, lines 36-38. Chung further teaches that a hole pattern is transferred into photoresist layer 130 through exposure. Column 4, lines 41-42. Chung further teaches that the hole pattern of photoresist layer 130 is transferred into cap layer 114 by using a conventional dry etch method and in-situ the photoresist layer 130 is removed by using O_2 plasma treatment in the same etcher. Column 4, lines 44-48. Chung further teaches that the hole pattern of cap layer 114 is transferred into two low k organic layers 112 and 113 including stop layer 116 by using any suitable conventional anisotropic dry etch method. Column 4, lines 49-52. Chung further teaches that having formed hole pattern in dual damascene, a trench is next formed. Column 4, lines 55-56. Chung further teaches that another photoresist layer 131 is formed and imaged line patterns with prior conditions. Column 4, lines 56-57. Chung further teaches that the line patterns of photoresist layer 131 is transferred into cap layer 114 by using a conventional dry etch method and in-situ the

photoresist layer 131 is removed by O_2 plasma treatment in the same etcher. Column 4, lines 58-61.

Applicants' Background, on the other hand, teaches a polysilicon layer is deposited on a thin insulating layer grown on the substrate. Specification, page 1, lines 15-16. Applicants' Background further teaches that a conventional SiON antireflective coating ("ARC") layer of a desired thickness is then deposited. Specification, page 1, lines 16-17. Applicants' Background further teaches that the first photoresist layer is then patterned on the conventional ARC layer. Specification, page 2, line 2. Applicants' Background further teaches that once the first photoresist pattern has been defined, the stack gates of the memory region are etched. Specification, page 2, lines 9-10. Applicants' Background further teaches that the first resist layer is then removed and residues cleaned using a wet etch. Specification, page 2, lines 10-11. Applicants' Background further teaches that a second photoresist pattern is defined. Specification, page 2, line 11. Applicants' Background further teaches that masking in the second photoresist layer defines gates in the logic region of the conventional imbedded memory while the second photoresist layer also covers the memory region to ensure that processing of the logic region does not affect the memory region. Specification, page 2, lines 14-17. Applicants' Background further teaches that the gates in the logic region are then etched. Specification, page 2, lines 17. Applicants' Background further teaches that the second photoresist layer may then be stripped and residues clean. Specification, page 2, lines 17-18.

By combining the damascene process, as taught in Chung, with the conventional method for processing a portion of a semiconductor device, as taught in Applicants' Background, Chung would no longer be able to etch low k organic dielectric film in a semiconductor device that substantially avoids the complicated process flow from spin-on low k organic dielectric layer. There are no low k organic dielectric layers taught in Applicants' Background. Further, there is no stop layer in between the two low k organic dielectric layers. Hence, Chung may no longer be able

to etch low k organic dielectric film which is the purpose of the operation of Chung. Thus, by combining Chung with Applicants' Background, the principal of operation in Chung would change, essentially render the operation of Chung to perform its purpose unsatisfactorily. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-6 and 18. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959); *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

II. ALLOWABLE SUBJECT MATTER:

Applicants appreciate the allowance of claims 13-17. Paper No. 8, page 5.

III. CONCLUSION:

As a result of the foregoing, it is asserted by Applicants that claims 1-6 and 13-18 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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EXHIBIT A

damascene	process in which interconnect metal lines are delineated in dielectrics isolating them from each other not by means of lithography and etching, but by means of chemical-mechanical planarization (CMP); in this process interconnect pattern is first lithographically defined in the layer of dielectric then metal is deposited to fill resulting trenches and then excess metal is removed by means of chemical-mechanical polishing (planarization).